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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/063,893	05/22/2002	Chung-Yuan Liu	CMOP0017USA	2372

27765 7590 11/19/2004

NAIPO (NORTH AMERICA INTERNATIONAL PATENT OFFICE)  
P.O. BOX 506  
MERRIFIELD, VA 22116

EXAMINER
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COLEMAN, WILLIAM D

ART UNIT	PAPER NUMBER
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2823

DATE MAILED: 11/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/063,893

Applicant(s)

LIU, CHUNG-YUAN

Examiner

W. David Coleman

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 30 September 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1 and 4-11 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1 and 4-11 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

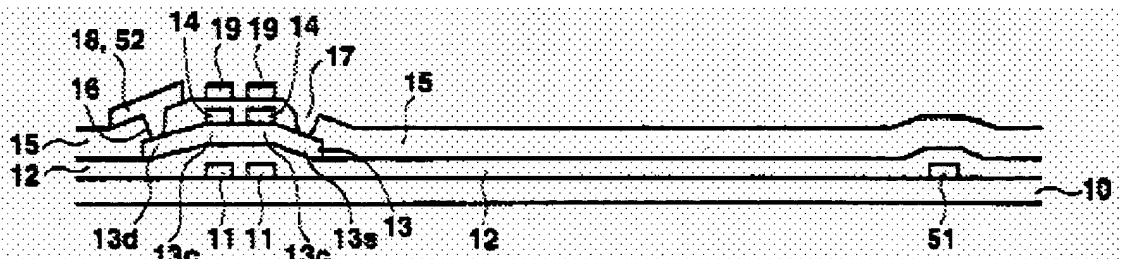
**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

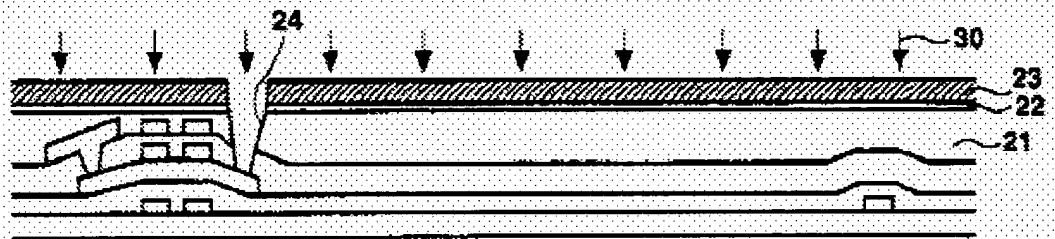
### ***Response to Arguments***

1. Applicant's arguments filed September 30, 2004 have been fully considered but they are not persuasive.
2. Applicants contend that amending claims 1, 5, 7 and 9 with the present amendment "simultaneously" forming at least one transistor "and a plurality of bumpy stacked structures" would render the Noritake et al., U.S. Patent 6,410,358 B1 herein known as Noritake moot.
3. In response to Applicants contention that the newly added terms "simultaneously" and "bumpy stacked structures", will obviate the Noritake prior art reference please see the following drawings where the bumpy stacked structures are formed simultaneously.



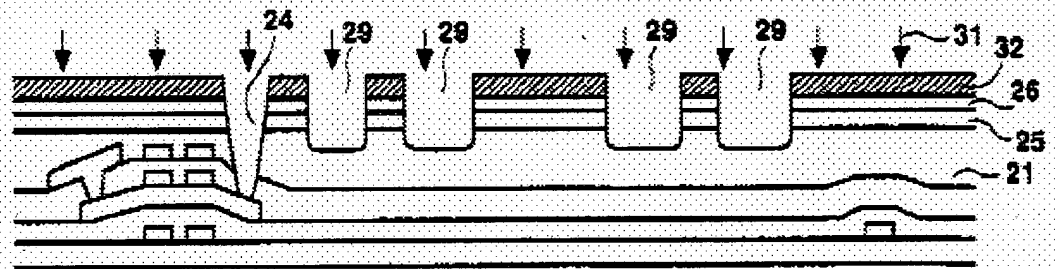
**Fig. 3(a)**

PRIOR ART



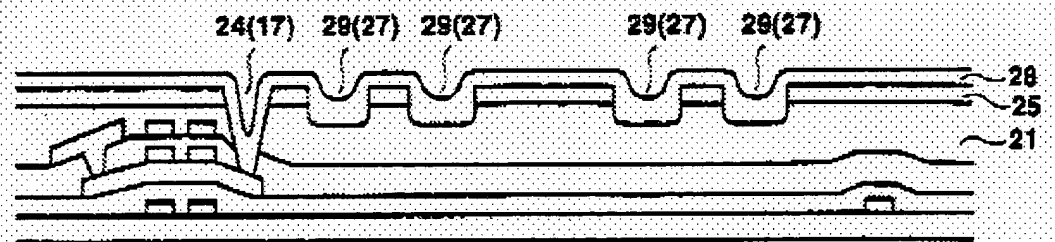
**Fig. 3(b)**

PRIOR ART



**Fig. 3(c)**

PRIOR ART



**Fig. 3(d)**

PRIOR ART

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4. Noritake discloses at least one transistor and a plurality of stacked structures having different widths. Please note that the gate signal line 51 and first gate electrode 11 will be formed simultaneously having a bumpy effect on the substrate (not numbered).

***Claim Rejections - 35 USC § 102***

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

5. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

6. Claims 1-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Noritake et al., U.S. Patent 6,410,358 B1.

Noritake discloses a semiconductor process as claimed. See **FIGS. 1(a)-4(e)**, where Noritake teaches the claimed limitations.

7. Pertaining to claim 1, Noritake teaches a method of manufacturing a reflector comprising:  
providing a substrate **10**;  
simultaneously forming at least one thin film transistor (not numbered) and a plurality of bumpy stacked structures on the substrate, each of the bumpy stacked structures comprising a plurality of sub-stacked layers which have at least two different widths;

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forming a thin film layer **26** for covering the thin film transistor and the plurality of bumpy stacked structures;

forming a contact hole (please note that a hole is formed in the S/D region) in the thin film layer; and depositing a reflective metal layer **28** on the thin film layer; wherein the reflective metal layer is electrically connected to the thin film transistor through the contact hole.

8. Pertaining to claim 4, Noritake teaches the method of claim 1 wherein the thin film layer is a laminated layer comprising a photoresist layer **22**, an organic layer **21**, and an inorganic passivation layer **15**.

9. Pertaining to claim 5, Noritake teaches the method of claim 4 wherein a method of forming the contact hole comprises:

forming the inorganic passivation layer **15** on the thin film transistor and the plurality of bumpy stacked structures;

forming the organic layer **21** on the inorganic passivation layer;

forming the photoresist layer **22** on the organic layer;

performing a photolithography process for forming a predetermined pattern in the photoresist layer (see figures **1a** and **1b**);

etching the organic layer and the inorganic passivation layer along the predetermined pattern so as to form the contact hole (as seen in **1c**);

removing the photoresist layer; and

performing a baking process for smoothening the organic layer (column 5, lines 9-11).

10. Pertaining to claim 6, Noritake teaches the method of claim 1 wherein the thin film layer is a laminated layer comprising an organic layer and an inorganic passivation layer, and the organic layer is made of a photoresist material.

11. Pertaining to claim 7, Noritake teaches the method of claim 6 wherein a method of forming the contact hole comprises:

forming the inorganic passivation layer **15** on the thin film transistor and the plurality of bumpy stacked structures;

forming the organic layer **70** on the inorganic passivation layer;

performing a photolithography process for forming a predetermined pattern in the organic layer;

etching the inorganic passivation layer along the predetermined pattern so as to form the contact hole; and

performing a baking process for smoothening the organic layer (as described above).

12. Pertaining to claim 8, Noritake teaches the method of claim 1 wherein the thin film layer is an organic passivation layer, which is made of a photoresist material (column 4, line 44, i.e., photosensitive resin).

13. Pertaining to claim 9, Noritake teaches the method of claim 8 wherein a method of forming the contact hole comprises:

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forming the organic passivation layer on the thin film transistor and the plurality of bumpy stacked structures;

performing an exposing process for forming a predetermined pattern in the organic passivation layer;

performing a developing process on the organic passivation layer so as to form the contact hole; and

performing a baking process for smoothening the organic passivation layer.

***Claim Rejections - 35 USC § 103***

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

15. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noritake et al., U.S. Patent 6,410,359 B1 in view of Yamazaki et al., U.S. Patent 6,429,059 B2.

16. Noritake discloses a semiconductor process substantially as claimed.

17. Pertaining to claim 10, Noritake teaches the method of claim 1 wherein each of the sub-stacked layers is formed from a material selected from the group consisting of an insulating layer, a gate electrode layer and a metal layer. However, Noritake fails to disclose a amorphous silicon layer, an N + silicon layer. Yamazaki teaches forming an amorphous silicon layer and an N+ silicon layer. See **FIGS. 1A-29**, where Yamazaki teaches forming an amorphous silicon layer. And an N+ layer in the formation of a liquid



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crystal display. In view of Yamazaki, it would have been obvious to one of ordinary skill in the art to incorporate the limitations of Yamazaki into the Noritake semiconductor process because an active matrix type display device having a driver circuit and a pixel matrix circuit as integrated on the substrate (column 24, lines 17-30, also note that film **3004** comprises an amorphous silicon layer and an N+ layer **39**).

18. Pertaining to claim 11, Noritake teaches the method of claim 1 wherein each of the sub-stacked layers is formed from a material selected from the group consisting of a gate electrode,

a common electrode, an insulating layer, a metal layer, a source electrode, a drain electrode, and a passivation layer. However, Noritake fails to disclose a amorphous silicon layer, an N + silicon layer. Yamazaki teaches forming an amorphous silicon layer and an N+ silicon layer. See **FIGS. 1A-29**, where Yamazaki teaches forming an amorphous silicon layer. And an N+ layer in the formation of a liquid crystal display. In view of Yamazaki, it would have been obvious to one of ordinary skill in the art to incorporate the limitations of Yamazaki into the Noritake semiconductor process because an active matrix type display device having a driver circuit and a pixel matrix circuit as integrated on the substrate (column 24, lines 17-30, also note that film **3004** comprises an amorphous silicon layer and an N+ layer **39**).

### ***Conclusion***

19. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

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20. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 571-272-1856. The examiner can normally be reached on 9:00 AM-5:00 PM.

22. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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23. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



W. David Coleman  
Primary Examiner  
Art Unit 2823

WDC